REMARKS

Formal acceptance of the above-amendments as a Submission in connection with USPTO RCE practice is respectfully requested.

With the above-made amendments, claims 1-48 are now pending of which claims 1-3, 6-8, 10 and 11 are currently amended. (Claims 12-44, 47 and 48 remain withdrawn for purposes for examination.)

Amendments were made to the claims for purposes for effecting further clarification of the invention intended to be covered including in terms of more clearly defining the claims over the art documents cited in the outstanding rejections.

According to the final Office Action, claims 1-8, 10 and 11 and 45-46 stand rejected under 35 USC 103(a) as unpatentable over Huang (US 6,406,987), previously of record, in view of Huang, et al. (US 6,235,606), newly cited; claim 9 stands rejected under 35 USC 103 over the combination of Huang, as applied to the aforesaid claims, and further in view of Nishioka (US 2002/0008019), of record; claims 1-8, 10-11 and 45-46 were also rejected under 35 USC 103(a) over the combination of Lee (US 6,184,071), newly cited, in view of Huang, et al. ('606); and claim 9 stands rejected under 35 USC 103 over the combination of Lee (supra) in view of Nishioka. As will be shown below, the invention according to these claims could not have been rendered obvious in the manner alleged in these rejections. Therefore, insofar as presently applicable, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

A key aspect of the invention pertains to the height of the insulating film which is embedded in the trench associated with the element isolating region (e.g., STI). In accordance with the invention in each of the independent claims 1, 6-8, 10 and 11, the recessed height of the embedding insulating film that is deposited on the element

isolation trench is at a depth, extended from the plane surface of the semiconductor substrate (where the gate electrode is formed), substantially the same as or greater than that of the source and drain diffusion regions. In this regard, the last "wherein" clause in independent claim 1 was revised so that it now reads:

> "wherein the plane of said second edge surface of said embedding insulating film is positioned at a depth, extended from a plane surface of said semiconductor substrate, substantially the same as or greater than that of said source and drain diffusion regions."

This can be seen with regard to Figs. 1E-1H as well as the discussion with regard to Figs. 2-16 of the drawings. By effecting a scheme such as that set forth in base claim 1 as well as in the corresponding dependent claims, the recessed height of the embedding insulating layer inside the trench is as deep or is deeper than the source/drain regions so that the stress that would otherwise be caused by the presence of the insulating film near the source and drain regions is ameliorated. As a result, the crystalline defects are suppressed in the semiconductor element.

Similar such featured aspects, in effect, are now also contained, although they may be presented somewhat differently, in each of the other independent claims, i.e., claims 6, 7, 8, 10 and 11. A minor clarification was also effected in dependent claim 2, and with regard to dependent claim 3 the language therein was revised to conform to the revisions implemented in the corresponding base claim 1. It is submitted, the invention as now set forth in claims 1-11 as well as in claims 45 and 46, both of which depend on claim 1, could not have been achievable in the manner as that alleged in the outstanding rejections.

Crystalline defects are sometimes caused in the element isolation region by the stress caused from the element isolation region (e.g., STI stress), the stress resulting from the implanted impurities in the active region such as in connection with the formation of the source and drain regions of a MOS transistor, *et seq*. For example, the growth of the oxide film on the side wall of the trench leads to volume expansion of, for example, silicon oxide (SiO_2) by the heat treatment after the element isolating insulating film is embedded in the STI trench. When silicon (Si) is changed into SiO_2, a volume expansion of SiO_2 may become two or more times larger than the volume expansion of Si. Since such volume expansion is restrained by the presence of the embedded oxide film (e.g., 103), this causes even higher compression stresses (STI stresses) in the substrate which may lead to crystalline defects in the device, such as shown with regard to the discussion of Figs. 2-3 and 4-5. Extensive discussion regarding this can be found on pages 34-41 of the Substitute Specification (similarly also in the original submitted specification).

Regarding the "first edge surface" and that of the "second edge surface" of the "embedding insulating film" in the trench, supportive discussion regarding this can be found with regard to Figs. 9 and 10 of the drawings, in connection with the description of the formation of the embedding insulating film 103 (see Fig. 1D et seq.), and page 29 of the specification, as well as the related discussion of stresses associated with the formation of the STI (Shallow Trench Isolation) region, e.g., in conjunction with the impurity-caused stress associated with the formation of the ion implanted source and drain diffusion regions of the MOS transistors.

Huang ('987) as well as Huang, et al. ('606) disclosed the STI. However, neither Huang ('987) or Huang, et al. ('606) disclosed or suggested a recessed

height (depth) to the degree of specificity to which the present invention demands. Additional discussion regarding Huang ('987) can be found in the remarks of the amendment dated July 23, 2004, which is incorporated herein for the purpose of this response. It is submitted, there would have been no reason for either Huang or Huang, et al. to have designed their scheme with the same specificity regarding the embedding insulating film since there is no evidence that either of them were concerned with the problems to which the present inventors addressed, which problems are extensively discussed in the present specification.

With regard to Lee's disclosed device and method therefor, it is observed that the upper plane surface of the buried insulating film 39 is vertically at a higher level than that of either of the source or drain regions. In Nishioka, moreover, the silicon oxide film 106, it is observed, extends to a higher plane than that of the source and drain of MOS memory cell transistor. In fact, Applicants submit, both Lee and Nishioka taught an entirely different construction than that according to the invention, as now set forth in claims 1-11 and 45 and 46. It is submitted, also, even if one of ordinary skill in the art would attempt to apply the teachings of the cited references (in the outstanding rejections) in any combination, there still could not have been devised a semiconductor device construction as that presently set forth. That is, there is no teaching or suggestion by any combination of these references that would have led to a construction as that now set forth in claims 1-11, 45 and 46. It is submitted, at least for the above reasons, the invention according to claims 1-11, 45 and 46 could not have been rendered obvious, as alleged in the outstanding rejections.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, favorable action on this Submission and early allowance of the above-identified application is respectfully requested.

Applicants request any shortage of fees due in connection with the filing of this paper, including extension of time fees, be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 500.42877X00), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

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